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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,492	04/21/2004	Sadami Takeoka	60188-820	5291

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,492	TAKEOKA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-18* is/are pending in the application.

4a) Of the above claim(s) *17 and 18* is/are withdrawn from consideration.

5)☒ Claim(s) *14 and 15* is/are allowed.

6)☒ Claim(s) *11-13 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/187,269.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11,12,13, and 16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over JARWALA ET AL. (5,673,276) in view of KOMOIKE (6,094,736) and Yamamura (5,341,096).

Jarwala et al. disclose a semiconductor device comprising a semiconductor wiring substrate 10, said semiconductor wiring substrate 10 being composed of a ceramic, having a wiring ("leads," not shown for the sake of clarity, note column 3 line 53) layer; a plurality of chip IPs 14 mounted on said semiconductor wiring substrate 10 by being bonded thereto; a boundary scan test circuit 16 provided in each of said chip IPs 14; scanning signal input terminals 53' and 53 connected to an internal scan chain (note column 5 lines 62-65), at least one of said scanning signal input terminals 53' and 53 being a terminal 53 specially formed separately from said boundary scan test circuit 16; wherein said internal scan chain is for an internal scan test (such as described at

column 4 lines 36-47) provided in each of said chip IPs 14, and the boundary scan test circuit 16 and the internal scan chain for an internal scan test are formed so as to be capable of performing a boundary scan test and an internal scan test simultaneously with each other for testing said combinational ("combined out of constituent parts") circuit, using test data for an internal scan test which is input from outside. Note figures 3-6 and 9-12 of Jarwala et al.

Jarwala et al. do not disclose that said ceramic is semiconductor material. However, Komoike discloses a semiconductor wiring substrate 1 being composed of a semiconductor (note figure 1) on which a plurality of semiconductor chip IPs 2,4 are to be mounted; and a plurality of pieces of wiring 7 formed on the semiconductor substrate 1 to be used only for testing. Note figure 1 of Komoike. Why should one substitute the semiconductor substrate of Komoike for the ceramic substrate of Jarwala et al.? One having skill in the Multi-chip Module Art would know. A mismatch in the materials used for the substrate and the chips bonded thereon could result in a TCE (thermal coefficient of expansion) mismatch. When the assembly is heated, the substrate and chips could expand at different rates, resulting in potentially damaging stress between the constituent parts. This problem is often discussed in the art, for example at column 1 lines 17-40 of Canestaro et al. 4,728,751. Therefore, it would have been obvious to a person having skill in the art to replace the ceramic material of Jarwala et al.'s substrate with the semiconductor material such as taught by Komoike in order to match the

material, and thus the CTE, of the chip IPs to thus avoid possible damage due to thermal stress.

Further, Jarwala et al. does not disclose (at least in so many words. Given that Jarwala et al. discloses a test circuit it would make sense if Jarwala et al. also disclosed something to test, but Jarwala et al. leaves the test object to the reader's imagination) that said chip IPs each include a logic circuit which is a test object (DUT, which is "slang" for **D**evice **U**nder **T**est) to be tested by said internal scan test. However, Yamamura discloses a semiconductor device very similar to Jarwala et al.'s in that it includes a boundary scan test circuit 7b provided in each of a group of chip IPs 1A, 1B; and an internal scan chain 7a for an internal scan test, said scan chain being formed in each of said chip IPs 1A, 1B and capable of operating simultaneously with said boundary scan test circuit 7b. Note figures 2-5, 9, 12A, column 2 lines 11-21, and column 5 lines 11-57 of Yamamura. Yamamura also discloses a "logic circuit which is a test object (DUT)" in the form of testable LSI's (large scale integrated circuits in each of said chip IPs 1A, 1B, to be tested by Yamamura's internal scan test. Therefore, it would have been obvious to a person having skill in the art to augment Jarwala et al.'s semiconductor device with the logic circuit which is a test object (DUT, which is "slang" for **D**evice **U**nder **T**est) to be tested by said internal scan test such as taught by Yamamura in order to give the scan test something to test, to thus a valuable use for the scan test.

Allowable Subject Matter

2. Claims 14 and 15 are allowed over the art of record.

Response to Arguments

1. Applicant's arguments filed 07/06/2007 have been fully considered but they are not persuasive.

It is argued, at page 3 of the remarks that "One feature of the present invention is that it uses test data for an internal scan test which is input from outside." However, Jarwala et al.'s "TDI 18 of a separate one of the chips 14_2, 14_3... 14_n," note figure 4 of Jarwala et al., is structurally identical to Applicants' "pieces of wiring [TDI] branching off from the boundary scan test circuit 67 [that] are formed outside the in-chip chain formed by the boundary scan test circuit 67, and inputting of a test pattern for a scan test on the internal circuits and outputting of the scan test result are performed by using, through these wiring branches, the wiring for testing only," note figure 12 and paragraph 0127 of the instant application. The applicant's claim 11 cannot distinguish over a device including the "TDI 18" suggested by the Jarwala et al. reference simply on the basis of a function allegedly performed by the claimed device, because only the device per se is relevant, not the recited function of inputting data from outside.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. See *In re Ludtke,* 441

F2d 660, 664, 169 USPQ 563, 566 (1971), and *In re Swinehart,* 439 F.2d 210, 212-3, 169 USPQ 226, 229 (CCPA 1971), both of which make it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" terms or not. Note that the above caselaw makes clear that in such cases applicant has the burden of showing that a prior art device that appears reasonably capable of performing the allegedly novel function is in fact incapable of doing so. See MPEP § 2114. See also *In re Schreiber*, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997) (Claim to a spout having "taper ... such as to by itself jam up the popped popcorn before the end of the cone and permit the dispensing of only a few kernels at a shake," anticipated by an oil can spout having the same shape as spout Applicant disclosed as being adapted for dispensing said only a few kernels) and *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks") for discussions of the roles of examiner and applicant in determining when and how functional limitations distinguish a claim from prior art disclosing the same structure.

In this case it is reasonable to assume that Jarwala et al.'s device is capable of inputting data from outside, because of the structural similarity between Jarwala et al.'s

TDI 18 and Applicant's "pieces of wiring branching off the scan circuit [and] formed outside the in-chip chain."

Because it is reasonable to assume that assume that Jarwala et al.'s TDI 18 is capable of performing the claimed function, the burden shifts to Applicants to show that it is not. See MPEP § 2114.

Applicants may well have invented a method of performing novel non-obvious steps using a piece of equipment that was always suited for such use, but never actually used so. If so, the obviousness analysis of the claimed device is unaffected. Recall the traverse ("Schreiber argues, however, that Harz does not disclose that such a structure can be used to dispense popcorn from an open-ended popcorn container") put forth by the *In re Schreiber* appellant. The Federal Circuit replied:

> Although Schreiber is correct that Harz does not address the use of the disclosed structure to dispense popcorn, the absence of a disclosure relating to function does not defeat the Board's finding of anticipation. It is well settled that the recitation of a new intended use for an old product does not make a claim to that old product patentable. *See In re Spada*, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990) ("The discovery of a new property or use of a previously known composition, even when that property and use are unobvious from prior art, cannot impart patentability to claims to the known composition."); Titanium *Metals Corp. of Am.* v. *Banner,* 778 F.2d 775, 782, 227 USPQ 773, 778 (Fed. Cir. 1985) (composition claim reciting a newly discovered property of an old alloy did not satisfy section 102 because the alloy itself was not new); In *re Pearson,* 494 F.2d 1399, 1403, 181 USPQ 641, 644 (CCPA 1974) (intended use of an old composition does not render composition claim patentable); In *re Zierden,* 411 F.2d 1325, 1328, 162 USPQ 102, 104 (CCPA 1969) ("[M]ere statement of a new use for an otherwise old or obvious composition cannot render a claim to the composition patentable."); In *re Sinex*, 309 F.2d 488, 492, 135 USPQ 302, 305 (CCPA 1962) (statement of intended use in an apparatus claim failed to distinguish over the prior art apparatus); *In re Hack* , 245 F.2d 246, 248, 114 USPQ 161, 162 (CCPA 1957) ("the grant of a patent on a composition or a machine cannot be predicated on a new use of that machine or composition"); *In re Benner* , 174 F.2d 938, 942, 82 USPQ 49, 53 (CCPA 1949) ("no provision has been made in the patent statutes for granting a patent upon an old product based solely upon discovery of a new use for such product"). Accordingly, Schreiber's contention that his structure will be used to dispense popcorn does not have patentable weight if the structure is already known, regardless of whether it has ever been used in any way in connection with popcorn.

In re Schreiber, 44 USPQ2d 1429, 1431 (Fed. Cir, 1997)

Applicant argues further that, "It is alleged that Yamamura discloses that it is possible to operate the boundary scan test circuit and the internal scan chain simultaneously during an internal scan test, and a test object (DUT) in each of the chip IPs." However, no such allegation has been raised. It is merely alleged that Yamamura teaches the benefits of supplying a device under test (DUT) when building a test circuit such as the one Jarwala et al. builds.

It is argued, at page 3 of the remarks, that "However, Yamamura fails to disclose a semiconductor device that uses test data for an internal scan test which is input from outside. Yamamura discloses a circuit having a built-in self test (BIST) mechanism that when the boundary scan test circuit and the *internal* scan chain are simultaneously operated, a periodic pattern generated in an internal circuit and a random pattern data are used as test data (see, col. 6, lines 6-26 and col. 8, lines 36-57 of Yamamura). Thus, the test data is not input from the outside, but rather from the inside." This argument amounts to nothing more than an allegation that a particular device disclosed by one (but not all) of the references is not performing the process Applicant alleges to be novel. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208

USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant argues further that, "Furthermore, it is well known in the art, such as Yamamura, that LSIs have been configured so that a boundary scan test and a built-in self test can be operated simultaneously. However, the prior art also shows that LSIs cannot operate a boundary scan test and *an internal scan test* simultaneously during an internal scan test using data input from the outside. Thus, the object of Yamamura is different to that of the present invention. As such, it is clear that Yamamura fails to disclose the above cited limitation of claim 11." However, were the Examiner to find that the prior art I fact shows that LSIs cannot operate a boundary scan test and *an internal scan test* simultaneously during an internal scan test using data input from the outside, the Examiner would be required to make a finding[1] of fact. Findings of fact require objective evidence. Applicants' page 3 argument takes the form of attorney argument. The arguments of counsel cannot take the place of evidence in the record. *In re Schulze*, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965). See MPEP §§ 716.01(c), 2145.

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[1] This is the precise finding *Ludtke* court tells us the Examiner must find: that the device suggested by the prior art would have been incapable of performing the claimed function. See *Ludtke*, 169 USPQ at 567.

Conclusion

2. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

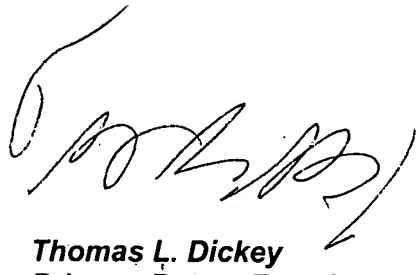
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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